COURSE DESCRIPTION CARD - SYLLABUS

Course name
Design verification in FPGA technology [S2EiT1-MIEPU>WPwFPGA]

Course

Field of study
Electronics and Telecommunications

Year/Semester
2/3

Area of study (specialization)
Multimedia and Consumer Electronics

Profile of study
general academic

Level of study
second-cycle

Course offered in
Polish

Form of study
full-time

Requirements
elective

Number of hours

Lecture
30

Laboratory classes
15

Other
0

Tutorials
0

Projects/seminars
0

Number of credit points

4,00

Coordinators

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Lecturers

Prerequisites

none

Course objective

none

Course-related learning outcomes

none

Methods for verifying learning outcomes and assessment criteria

Learning outcomes presented above are verified as follows:

none

Programme content

none

Course topics

none

Teaching methods

none

Bibliography

none

Breakdown of average student's workload

	Hours	ECTS
Total workload	100	4,00
Classes requiring direct contact with the teacher	58	2,00
Student's own work (literature studies, preparation for laboratory classes/ tutorials, preparation for tests/exam, project preparation)	42	2,00